PIC18F24K20/25K20/44K20/45K20 Silicon Errata and Data Sheet Clarification

The PIC18F24K20/25K20/44K20/45K20 devices that you have received conform functionally to the current Device Data Sheet (DS41303**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F24K20/25K20/44K20/45K20 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**AF**).

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F24K20/25K20/44K20/45K20 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1) (11-bit)	Revision ID for Silicon Revision(2) (5-bit)								
		A4	A7	A9	AB	A4	A7	A8	AE	AF
PIC18F24K20	105h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F25K20	103h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F44K20	104h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F45K20	102h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

2: Refer to the *"PIC18F2XK20/4XK20 Flash Memory Programming Specification"* (DS41297) for detailed information on Device and Revision IDs for your specific device.

3: Shaded cells in this table indicate older device revisions that are no longer in production.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)								
				A4	A7	A9	AB	A4	A7	A8	AE	AF
				0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
ECCP	CCP1CON	1.	Changing CCP1M bits may cause capture of Timer1 value.	X	X	X	X					
ECCP	Full-Bridge mode	2.	Direction change issue.	X	X	X	X					
MSSP SPI	SPI Clock	3.	Shortened SPI high time.	X	X	X	X					
MSSP I^2C™	Slew Rate	4.	Slow slew rate when SLRCON<2> is set.	X	X	X	X					
ADC	Offset	5.	Time dependent on offset.	X	X	X	X					
MSSP I^2C	Receiving	6.	Address may be received as data.	X	X	X	X					
MSSP I^2C	Master mode	7.	Master mode not functional.	X								
MSSP SPI	SPI Master	8.	Improper sampling of last bit.	X	X	X	X					
MSSP SPI	SPI Master	9.	$\overline{SS}$PBUF improperly reloads on $\overline{SS}$ pin transitions.	X	X	X	X					
MSSP SPI	SPI Master	10.	Improper extra pulse on SCK pin.	X	X	X	X					
EUSART	Synchronous Master mode	11.	Duty cycle of CK output is skewed when SPBRG is odd.	X	X	X	X					
EUSART	Synchronous Master mode	12.	LS bit corruption during transmission when SPBRG = 3.	X	X	X	X					
EUSART	Synchronous Master mode	13.	Clock fails to stop at end of character transmission when SPBRG = 0.	X	X	X	X					
Internal Fixed Voltage Reference (FVR)	—	14.	FVRST bit activates prematurely.	X	X							
High Low Voltage Detect (HLVD)	—	15.	IVRST bit activates prematurely.	X	X							
BOR	FVR	16.	Unexpected BOR occurrence.	X	X							
System Clocks	—	17.	HFINTOSC output accuracy.	X	X	X	X					
POR/BOR	—	18.	Unexpected code execution at low V_{DD}.	X	X	X	X					
POR	—	19.	Premature POR release.	X	X	X	X					
POR	—	20.	POR may become stuck.	X	X	X	X					
Clocks	EC mode	21.	48 MHz maximum frequency.	X	X							
Comparators	Interrupt-on-Change	22.	Presetting interrupt-on-change issue.	X	X	X	X					
Data EEPROM Memory	Endurance	23.	Endurance is limited to 10K cycles.	X	X	X	X	X	X	X		
Program Flash Memory	Endurance	24.	Endurance is limited to 1K cycles.	X	X	X	X	X	X	X		
Configuration Bits	CONFIG3H	25.	HFOFST bit erases to '0' instead of '1'.	X	X	X	X					

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

2: Shaded cells in this table indicate older device revisions that are no longer in production.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]								
				A4	A7	A9	AB	A4	A7	A8	AE	AF
				0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
EUSART	Asynchronous Receive mode	26.	RCIDL bit may stay low improperly.	X	X	X	X					
PORTB Interrupts	Interrupt-on-Change	27.	False interrupt when setting interrupt enable.	X	X	X	X	X	X	X	X	X
ADC	ADC Conversion	28.	ADC conversion may be limited to half scale.	X	X	X	X	X	X	X		
ECCP	Full-Bridge mode	29.	Wrong dead-band time.					X	X	X	X	X
ECCP	Full-Bridge mode	30.	Wrong signal start time.					X	X	X	X	X
MSSP SPI	SPI Clock	31.	Improper SCK output.					X	X	X	X	X
MSSP SPI	SPI Master	32.	Improper sampling of last bit.					X	X	X	X	X
MSSP SPI	SPI Master	33.	Improper handling of write collision.					X	X	X	X	X
MSSP I^2C™	I^2C™ Master	34.	Improper handling of Stop event.					X	X	X	X	X
EUSART	OERR Flag	35.	Clearing SPEN bit does not clear OERR flag.					X	X	X	X	X
EUSART	BAUDCTL	36.	RCIDL bit may stay low improperly.					X	X	X	X	X
PORTB Interrupts	Interrupt-on-Change	37.	False interrupt when waking from Sleep.					X	X	X	X	X
BOR	Reset	38.	Reset on configuring the analog comparators to the FVR.	X	X	X	X	X	X	X	X	X
Wake-up from Low-Power Sleep mode	Wake-up Sources	39.	Device may not wake-up under specific conditions.	X	X	X	X	X	X	X	X	X
Low-Voltage Detect	LVD in Sleep	40.	LVD erroneously triggers upon wake-up from Sleep if band gap is disabled in Sleep mode.	X	X	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

2: Shaded cells in this table indicate older device revisions that are no longer in production.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all specified revisions of silicon.

2: Shaded cells in this section indicate latest silicon in production.

1. Module: ECCP

Changing the CCP1M<3:0> bits of CCP1CON may cause the CCPR1H and CCPR1L registers to capture the value of Timer1.

Work around

Halt Timer1 before changing ECCP mode. Reload Timer1 with desired value after ECCP is setup and before Timer1 is restarted.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

2. Module: ECCP

Changing direction in Full-Bridge mode does not insert dead time between changing the active drivers in common legs of the bridge.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

4. Module: MSSP I²C™

Slew rate is slower than I²C specifications when the SLRCON<2> bit is set.

Work around

Clear SLRCON<2> bit when using the I²C peripheral.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

5. Module: ADC

Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time-dependent component (~2 LSb).

Work around

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms then take two ADC conversions and discard the first.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

6. Module: MSSP I²C

If a new address byte is received while the BF flag is set, the SSPOV bit is properly set and an ACK is not properly generated. If only the SSPOV bit is set (BF flag was cleared) and a matching address is clocked in, that received byte will be improperly loaded into the SSPBUF register and an ACK will be improperly generated.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

7. Module: MSSP I²C

I²C Master mode is not functional (Rev. A4 only).

Work around

Use software to emulate Master mode.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X								

8. Module: MSSP SPI

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

9. Module: MSSP SPI

In SPI Master mode, when CKE bit is set, the SSPBUF will reload the SSPSR output shift register on every high-to-low transition of the $\overline{SS}$ pin.

Work around

Avoid using the $\overline{SS}$ pin when the CKE bit is set and the MSSP is configured for SPI Master mode.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

10. Module: MSSP SPI

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

Work around

Configure SCK pin as an input until after the MSSP is setup.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

11. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to an odd number, the duty cycle of the CK output will be skewed by one baud clock count.

Work around

High values of SPBRG will minimize the effect of this anomaly.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

12. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to 3 and the TXREG is written while the previous character is still in the TX shift register, the LS bit of the TXREG character may be corrupted during transmission.

Work around

When SPBRG is set to 3, wait until the TRMT bit of the TXSTA register is set before loading TXREG with the next character to be transmitted.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

13. Module: EUSART

In Synchronous Master mode, if the SPBRG register is equal to 0 when the TXEN bit is set, then writing to TXREG will properly start transmission. However, the clock will be improperly out of phase with the data bits and the clock will not stop at the end of the character transmission.

Work around

Set SPBRG register to non-zero value before setting the TXEN bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

14. Module: Internal Fixed Voltage Reference (FVR)

The FVRST bit of the CVRCON2 register activates prematurely (Rev. A4 and A7 only).

Work around

Wait an additional 20 µs after FVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low-Voltage Detect, and the HFINTOSC.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

15. Module: High Low Voltage Detect (HLVD)

The IVRST bit of the HLVDCON register activates prematurely (Rev. A4 and A7 only).

Work around

Wait an additional 20 µs after IVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low-Voltage Detect, and the HFINTOSC.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

16. Module: BOR

An unexpected Brown-out Reset may occur when the fixed voltage reference is inactive and BOR is activated, thereby activating the fixed voltage reference simultaneously. This error is caused by a premature FVRST stable flag (Rev. A4 and A7 only) and only affects Brown-out disable in Sleep and software enabled BOR modes.

Work around

Enable the FVR by setting the FVREN bit of the CVRCON2 register and then wait an additional 20 µs after FVRST is sensed high before enabling BOR. Brown-out disable in Sleep mode with automatic enable on wake-up cannot be used.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

17. Module: System Clocks

HFINTOSC output frequency is 16 MHz ±3%, 25°C to 85°C.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

18. Module: POR/BOR

The POR rearm voltage may be below the low end of the BOR range, causing unexpected code execution below the BOR range.

Work around

Use external power monitor to hold the device in Reset below 1.1V.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

19. Module: POR

The POR may release around 0.8V (below the POR rearm voltage of 1.2V, nominal) when VDD rises from below 0.60V (when BOR is not enabled) or 0.33V (when BOR is enabled).

Work around

Use Power-up Timer when operating with the EC, EXTRC or HFINTOSC oscillator modes. Ensure that VDD rise time is less than the Power-up Timer time.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

20. Module: POR

The part may hang in the Reset state when VDD rises to the operating range at a rate faster than 7500V per second. Recovery from the hung state is possible only by first lowering VDD to below 0.3V, followed by raising VDD to the operating range.

Work around

Slow VDD rise time by adding series resistance between the voltage supply and the VDD pin and increasing the VDD bypass capacitance. VDD bypassing should remain on the pin side of the series resistor.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

21. Module: Clocks

EC mode operation is limited to a maximum of 48 MHz (Rev. A4 and A7 only).

Work around

Divide external clock by 4 and use HS-PLL Clock mode for external clocking above 48 MHz.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

22. Module: Comparators

When the CxON bit is clear, the output from the comparator will be properly forced to zero, but the CxPOL bit will improperly have no effect on the CxOUT bit. This prevents presetting the comparator change-on-interrupt mismatch latches as described in the data sheet.

Work around

Configure one of the unused comparator input channels as a digital output. Use that digital output to manipulate the comparator output to the desired CxOUT non-interrupt level. When the comparator is then set to the desired inputs, the mismatch latches will be preset to the non-interrupt level and the CxIF flag can then be cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

23. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

24. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

Work around

For data tables in program Flash memory use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

25. Module: Configuration Bits

Bit 3 of CONFIG3H defaults to '0' after a Bulk Erase instead of '1' as specified in the data sheet.

Work around

Program the HFOFST bit to the desired state after a Bulk Erase. All MPLAB® IDE programming tools currently perform this way.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

26. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/8th of a bit time is received. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

27. Module: PORTB

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration, then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

28. Module: ADC

After extended stress, the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are, instead, pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for V_{DD} = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low V_{DD} and decreases as V_{DD} increases.

Work around

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

29. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

30. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2 Prescale * DC1B[1:0].

Work around

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

31. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written, the SCK output is improperly immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

32. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

33. Module: MSSP SPI

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

Work around

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSPBUF register. In the event that a write collision does occur, use the slave select feature to resynchronize the slave clock.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

34. Module: MSSP I²C™

In Master I²C Receive mode if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. If a Start condition occurs after the improper Stop condition then 9 additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

35. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

36. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit, then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

37. Module: Interrupt-on-Change

When any interrupt-on-change is enabled and the corresponding input is high, then waking from Sleep by a source other than interrupt-on-change may cause the RBIF interrupt flag bit to become set improperly.

Work around

1. Use the INTx interrupt in lieu of interrupt-on-change.

Or

2. Store the state of the PORTB inputs before entering Sleep. Upon waking, if an RBIF is detected, then compare the PORTB levels with those stored. If they are the same, then clear and ignore the RBIF interrupt.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
				X	X	X	X	X

38. Module: BOR

An unexpected Brown-out Reset may occur when enabling the comparator with the Fixed Voltage Reference (FVR) selected as the V_{IN}+ input.

Work around

Disconnect the FVR from the V_{IN}+ comparator inputs prior to enabling the comparator and then reconnect it after enabling the comparator.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

39. Module: Wake-up from Low-Power Sleep mode

The device may not wake from Sleep when both of the following conditions are met:

1. The device is in Sleep mode for <1 ms;
2. On waking, the device executes a SLEEP instruction within 100 µs.

Under these conditions, the oscillator may stop before completing execution of the SLEEP instruction. The device will enter Sleep mode but will not wake-up on any enabled wake-up event, including the Watchdog Timer.

Work around

1. Disable High-Speed Start-up

Disabling High-Speed Start-up in the Configuration Word will delay the device executing code on wake-up by 250 µs, nominally, allowing the oscillator to stabilize.

The wake-up time from Sleep will increase by about 250 µs, nominally.

2. BOR enabled during Sleep

Configuring the device for hardware only BOR or software-controlled BOR and enabling SBOREN, the voltage reference is on during Sleep.

The device will wake-up and the oscillator will be stable. This will add 20 µA (nominal) to the Sleep current.

3. Enable the FVR during Sleep

In the same manner as the BOR, the FVR will keep the voltage reference on during Sleep, causing the oscillator to be stable on wake-up.

4. Avoid executing SLEEP within 100 µs of any wake-up event

This can be achieved by adding more instructions (NOP) before executing the SLEEP instruction. This minimizes the probability of the SLEEP instruction only partially executing.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

40. Module: Low-Voltage Detect

If Low-Voltage Detect is enabled, the band gap is disabled in Sleep, and the part is put to Sleep for a short period of time, the LVD will trigger immediately upon waking-up from Sleep.

Work around

Do not disable the band gap in Sleep when using the LVD.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

Data Sheet Clarifications

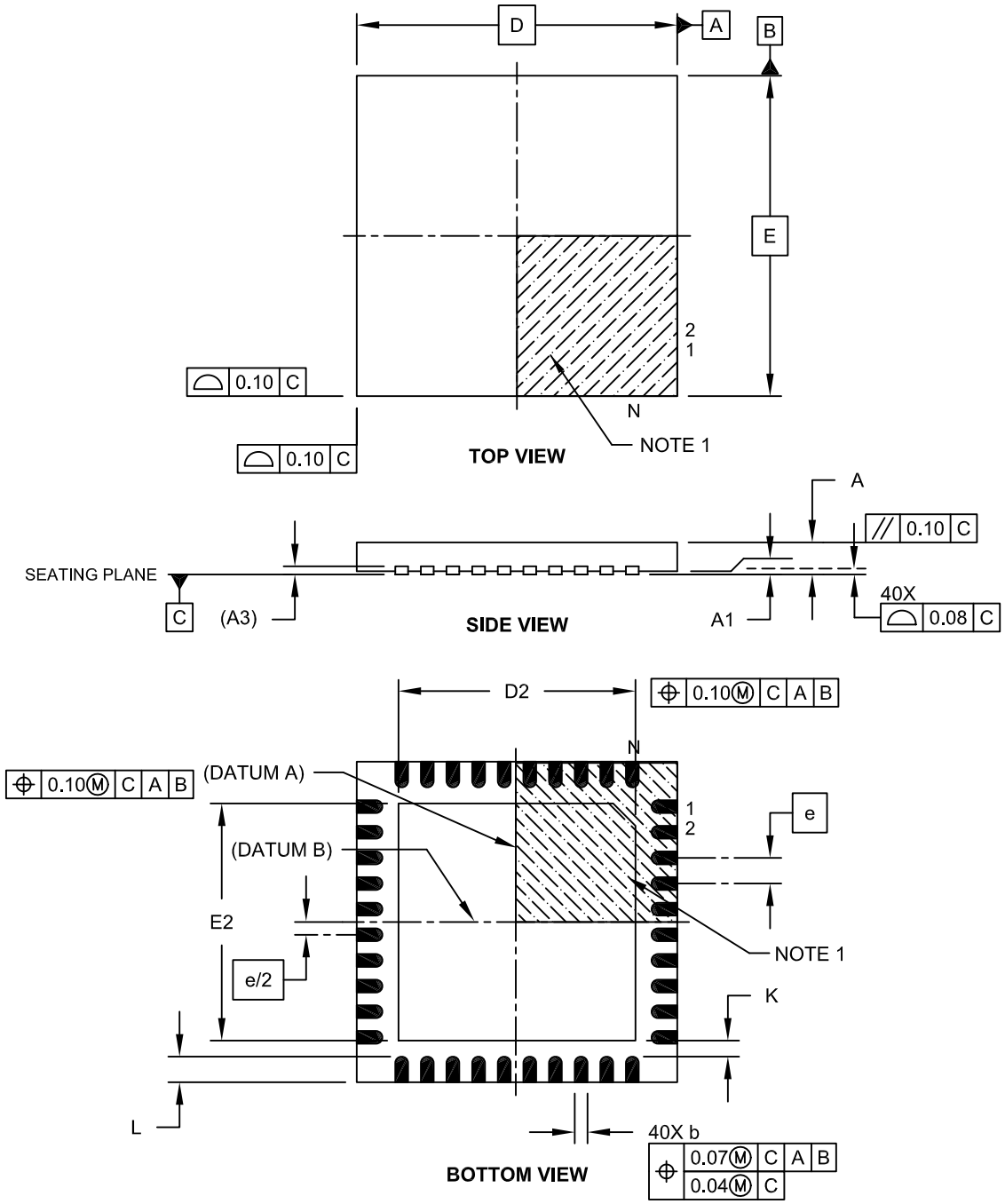
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303**G**):

1. Module: Dimensions for UQFN Packaging Option

The packaging information for the 40-pin UQFN is the following:

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

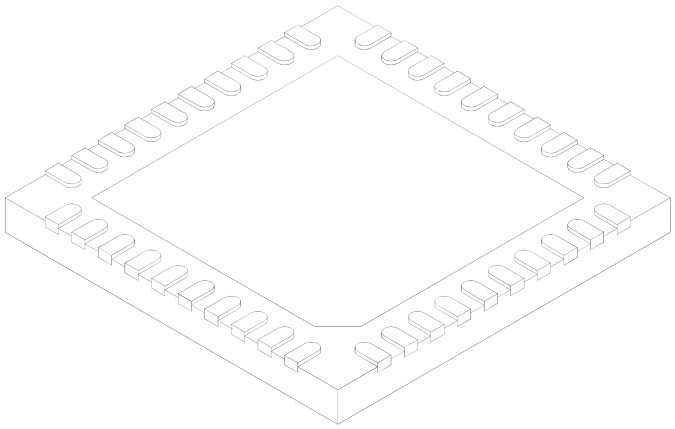
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2

2. Module: Electrical Characteristics

Parameter D026 in Table 26-8 on page 376 of the data sheet lists the maximum ADC delta current at 1.8V as 290 µA. The correct value should be 360 µA (correction in bold in Table 26-8).

TABLE 26-8: DC CHARACTERISTICS: PERIPHERAL SUPPLY CURRENT, PIC18F2XK/4XK20

PIC18F2XK20/4XK20		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
	Module Differential Currents						
D024 (ΔIWDT)	**Watchdog Timer**	0.7	2.0	µA	-40°C to +125°C	VDD = 1.8V	
		1.1	3.0	µA	-40°C to +125°C	VDD = 3.0V	
D024A (ΔIBOR)	**Brown-out Reset(2)**	21	50	µA	-40°C to +125°C	VDD = 2.0V	
		25	60	µA	-40°C to +125°C	VDD = 3.3V	
		0	—	µA	-40°C to +125°C	VDD = 3.3V	Sleep mode, BOREN<1:0> = 10
D024B (ΔIHLVD)	**High/Low-Voltage Detect(2)**	13	30	µA	-40°C to +125°C	VDD = 1.8-3.0V	
D025 (ΔIOSCB) LP	**Timer1 Oscillator**	0.5	2.0	µA	-40°C	VDD = 1.8V	32 kHz on Timer1(1)
		0.5	2.0	µA	+25°C		
		0.7	2.0	µA	+85°C		
		0.7	3.0	µA	-40°C	VDD = 3.0V	32 kHz on Timer1(1)
		0.7	3.0	µA	+25°C		
		0.9	3.0	µA	+85°C		
D025A (ΔIOSCB) HP	**Timer1 Oscillator**	11	30	µA	-40°C	VDD = 1.8V	32 kHz on Timer1(3)
		13	33	µA	+25°C		
		15	35	µA	+85°C		
		14	33	µA	-40°C	VDD = 3.0V	32 kHz on Timer1(3)
		17	37	µA	+25°C		
		19	40	µA	+85°C		
D026 (ΔIAD)	**A/D Converter(4)**	200	**360**	µA	-40°C to +125°C	VDD = 1.8V	A/D on, not converting
		260	**500**	µA	-40°C to +125°C	VDD = 3.0V	
ΔIFRC		2	5	µA	-40°C to +125°C	VDD = 1.8V	Adder for FRC
		11	18	µA	-40°C to +125°C	VDD = 3.0V	

Note 1: Low-Power mode on T1 osc. Low-Power mode is limited to 85°C.

2: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

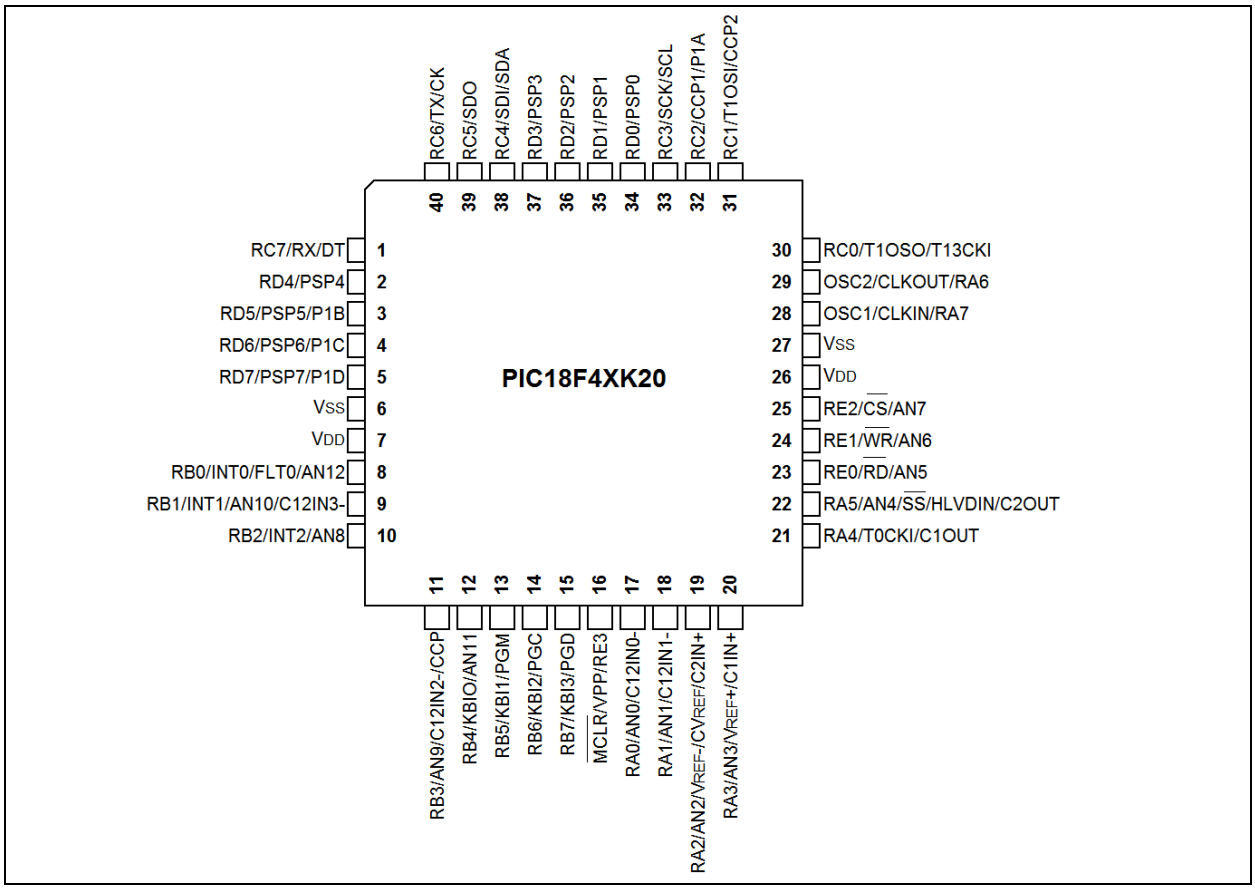
3: High-Power mode in T1 osc.

4: A/D converter differential currents apply only in Run mode. In Sleep or Idle mode both the ADC and the FRC turn off as soon as conversion (if any) is complete.

3. Module: Pin Diagram 40-pin UQFN

A new 40-pin UQFN diagram has been added to the data sheet (see Figure 26-1).

FIGURE 26-1: 40-PIN DIAGRAM UQFN



4. Module: PIC18F4XK20 Pin Summary

In Table 1 on page 7 of the data sheet, a new column that follows the QFN column has been added, as shown in bold in Table 1.

TABLE 1: PIC18F4XK20 PIN SUMMARY

DIL Pin	TQFP Pin	QFN Pin	**UQFN Pin**	I/O	Analog	Comparator	Reference	ECCP	EUSART	MSSP	Timers	Slave	Interrupts	Pull-up	Basic
2	19	19	**17**	RA0	AN0	C12IN0-	—	—	—	—	—	—	—	—	—
3	20	20	**18**	RA1	AN1	C12IN1-	—	—	—	—	—	—	—	—	—
4	21	21	**19**	RA2	AN2	C2IN+	VREF-/ CVREF	—	—	—	—	—	—	—	—
5	22	22	**20**	RA3	AN3	C1IN+	VREF+	—	—	—	—	—	—	—	—
6	23	23	**21**	RA4	—	C1OUT	—	—	—	—	T0CKI	—	—	—	—
7	24	24	**22**	RA5	AN4	C2OUT	HLVDIN	—	—	$\overline{SS}$	—	—	—	—	—
14	31	33	**29**	RA6	—	—	—	—	—	—	—	—	—	—	OSC2/ CLKOUT
13	30	32	**28**	RA7	—	—	—	—	—	—	—	—	—	—	OSC1/ CLKIN
33	8	9	**8**	RB0	AN12	—	—	FLT0	—	—	—	—	INT0	Yes	—
34	9	10	**9**	RB1	AN10	C12IN3-	—	—	—	—	—	—	INT1	Yes	—
35	10	11	**10**	RB2	AN8	—	—	—	—	—	—	—	INT2	Yes	—
36	11	12	**11**	RB3	AN9	C12IN2-	—	CCP2(1)	—	—	—	—	—	Yes	—
37	14	14	**12**	RB4	AN11	—	—	—	—	—	—	—	KBI0	Yes	—
38	15	15	**13**	RB5	—	—	—	—	—	—	—	—	KBI1	Yes	PGM
39	16	16	**14**	RB6	—	—	—	—	—	—	—	—	KBI2	Yes	PGC
40	17	17	**15**	RB7	—	—	—	—	—	—	—	—	KBI3	Yes	PGD
15	32	34	**30**	RC0	—	—	—	—	—	—	T1OSO/ T13CKI	—	—	—	—
16	35	35	**31**	RC1	—	—	—	CCP2(2)	—	—	T1OSI	—	—	—	—
17	36	36	**32**	RC2	—	—	—	CCP1/ P1A	—	—	—	—	—	—	—
18	37	37	**33**	RC3	—	—	—	—	—	SCK/ SCL	—	—	—	—	—
23	42	42	**38**	RC4	—	—	—	—	—	SDI/ SDA	—	—	—	—	—
24	43	43	**39**	RC5	—	—	—	—	—	SDO	—	—	—	—	—
25	44	44	**40**	RC6	—	—	—	—	TX/CK	—	—	—	—	—	—
26	1	1	**1**	RC7	—	—	—	—	RX/DT	—	—	—	—	—	—
19	38	38	**34**	RD0	—	—	—	—	—	—	—	PSP0	—	—	—
20	39	39	**35**	RD1	—	—	—	—	—	—	—	PSP1	—	—	—
21	40	40	**36**	RD2	—	—	—	—	—	—	—	PSP2	—	—	—
22	41	41	**37**	RD3	—	—	—	—	—	—	—	PSP3	—	—	—
27	2	2	**2**	RD4	—	—	—	—	—	—	—	PSP4	—	—	—
28	3	3	**3**	RD5	—	—	—	P1B	—	—	—	PSP5	—	—	—
29	4	4	**4**	RD6	—	—	—	P1C	—	—	—	PSP6	—	—	—
30	5	5	**5**	RD7	—	—	—	P1D	—	—	—	PSP7	—	—	—
8	25	25	**23**	RE0	AN5	—	—	—	—	—	—	$\overline{RD}$	—	—	—

TABLE 1: PIC18F4XK20 PIN SUMMARY

DIL Pin	TQFP Pin	QFN Pin	UQFN Pin	I/O	Analog	Comparator	Reference	ECCP	EUSART	MSSP	Timers	Slave	Interrupts	Pull-up	Basic
9	26	26	**24**	RE1	AN6	—	—	—	—	—	—	$\overline{WR}$	—	—	—
10	27	27	**25**	RE2	AN7	—	—	—	—	—	—	$\overline{CS}$	—	—	—
1	18	18	**16**	RE3**(3)**	—	—	—	—	—	—	—	—	—	—	$\overline{MCLR}$/ V_{PP}
11	7	7	**7**	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
32	28	28	**26**	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
12	6	6	**6**	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
31	29	30	**27**	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
–	NC	8	**—**	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
–	NC	29	**—**	—	—	—	—	—	—	—	—	—	—	—	V_{DD}

Note 1: CCP2 multiplexed with RB3 when CONFIG3H<0> = 0
2: CCP2 multiplexed with RC1 when CONFIG3H<0> = 1
3: Input-only.

5. Module: PIC18F4XK20 Pinout I/O Descriptions

In Table 1-3 on page 20 of the data sheet, a new UQFN column that follows the TQFP column has been added, as shown in bold in Table 1-3.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
$\overline{MCLR}$/VPP/RE3	1	18	18	**16**			Master Clear (input) or programming voltage (input)
$\overline{MCLR}$					I	ST	Active-low Master Clear (device Reset) input
VPP					P		Programming voltage input
RE3					I	ST	Digital input
OSC1/CLKIN/RA7	13	32	30	**28**			Oscillator crystal or external clock input
OSC1					I	ST	Oscillator crystal input or external clock source input
CLKIN					I	CMOS	ST buffer when configured in RC mode; analog otherwise
RA7					I/O	TTL	External clock source input. Always associated with pin function OSC1 (See related OSC1/CLKIN, OSC2/CLKOUT pins)
							General purpose I/O pin
OSC2/CLKOUT/RA6	14	33	31	**29**			Oscillator crystal or clock output
OSC2					O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode
CLKOUT					O	—	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
RA6					I/O	TTL	General purpose I/O pin

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
							PORTA is a bidirectional I/O port.
RA0/AN0/C12IN0-	2	19	19	**17**			
RA0					I/O	TTL	Digital I/O
AN0					I	Analog	Analog input 0, ADC channel 0
C12IN0-					I	Analog	Comparator C1 and C2 inverting input
RA1/AN1/C12IN0-	3	20	20	**18**			
RA1					I/O	TTL	Digital I/O
AN1					I	Analog	Analog input 1, ADC channel 1
C12IN0-					I	Analog	Comparator C1 and C2 inverting input
RA2/AN2/V_{REF-}/CV_{REF}/C2IN+	4	21	21	**19**			
RA2					I/O	TTL	Digital I/O
AN2					I	Analog	Analog input 2, ADC channel 2
V_{REF-}					I	Analog	A/D reference voltage (low) input
CV_{REF}					O	Analog	Comparator reference voltage output
C2IN+					I	Analog	Comparator C2 non-inverting input
RA3/AN3/V_{REF+}/C1IN+	5	22	22	**20**			
RA3					I/O	TTL	Digital I/O
AN3					I	Analog	Analog input 3, ADC channel 3
V_{REF+}					I	Analog	A/D reference voltage (high) input
C1IN+					I	Analog	Comparator C1 non-inverting input
RA4/T0CKI/C1OUT	6	23	23	**21**			
RA4					I/O	ST	Digital I/O
T0CKI					I	ST	Timer0 external clock input
C1OUT					O	CMOS	Comparator C1 output
RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT	7	24	24	**22**			
RA5					I/O	TTL	Digital I/O
AN4					I	Analog	Analog input 4, ADC channel 4
$\overline{SS}$					I	TTL	SPI slave select input
HLVDIN					I	Analog	High/Low-Voltage Detect input
C2OUT					O	CMOS	Comparator C2 output
RA6				**29**			See the OSC2/CLKOUT/RA6 pin
RA7				**28**			See the OSC1/CLKIN/RA7 pin

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on each input.
RB0/INT0/FLT0/AN12	33	9	8	**8**			
RB0					I/O	TTL	Digital I/O
INT0					I	ST	External interrupt 0
FLT0					I	ST	PWM Fault input for Enhanced CCP1
AN12					I	Analog	Analog input 12, ADC channel 12
RB1/INT1/AN10/ C12IN3-	34	10	9	**9**			
RB1					I/O	TTL	Digital I/O
INT1					I	ST	External interrupt 1
AN10					I	Analog	Analog input 10, ADC channel 10
C12IN3-					I	Analog	Comparator C1 and C2 inverting input
RB2/INT2/AN8	35	11	10	**10**			
RB2					I/O	TTL	Digital I/O
INT2					I	ST	External interrupt 2
AN8					I	Analog	Analog input 8, ADC channel 8
RB3/AN9/C12IN2-/ CCP2	36	12	11	**11**			
RB3					I/O	TTL	Digital I/O
AN9					I	Analog	Analog input 9, ADC channel 9
C12IN23-					I	Analog	Comparator C1 and C2 inverting input
CCP2(2)					I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output
RB4/KBI0/AN11	37	14	14	**12**			
RB4					I/O	TTL	Digital I/O
KBI0					I	TTL	Interrupt-on-change pin
AN11					I	Analog	Analog input 11, ADC channel 11
RB5/KBI1/PGM	38	15	15	**13**			
RB5					I/O	TTL	Digital I/O
KBI1					I	TTL	Interrupt-on-change pin
PGM					I/O	ST	Low-Voltage ICSP™ Programming enable pin
RB6/KBI2/PGC	39	16	16	**14**			
RB6					I/O	TTL	Digital I/O
KBI2					I	TTL	Interrupt-on-change pin
PGC					I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin
RB7/KBI3/PGD	40	17	17	**15**			
RB7					I/O	TTL	Digital I/O
KBI3					I	TTL	Interrupt-on-change pin
PGD					I/O	ST	In-Circuit Debugger and ICSP™ programming data pin

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
							PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32	**30**			
RC0					I/O	ST	Digital I/O
T1OSO					O	—	Timer1 oscillator output
T13CKI					I	ST	Timer1/Timer3 external clock input
RC1/T1OSI/CCP2	16	35	35	**31**			
RC1					I/O	ST	Digital I/O
T1OSI					I	CMOS	Timer1 oscillator input
CCP2(1)					I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output
RC2/CCP1/P1A	17	36	36	**32**			
RC2					I/O	ST	Digital I/O
CCP1					I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output
P1A					O	—	Enhanced CCP1 output
RC3/SCK/SCL	18	37	37	**33**			
RC3					I/O	ST	Digital I/O
SCK					I/O	ST	Synchronous serial clock input/output for SPI mode
SCL					I/O	ST	Synchronous serial clock input/output for I^2C™ mode
RC4/SDI/SDA	23	42	42	**38**			
RC4					I/O	ST	Digital I/O
SDI					I	ST	SPI data in
SDA					I/O	ST	I^2C™ data I/O
RC5/SDO	24	43	43	**39**			
RC5					I/O	ST	Digital I/O
SDO					O	—	SPI data out
RC6/TX/CK	25	44	44	**40**			
RC6					I/O	ST	Digital I/O
TX					O	—	EUSART asynchronous transmit
CK					I/O	ST	EUSART synchronous clock (see related RX/DT)
RC7/RX/DT	26	1	1	**1**			
RC7					I/O	ST	Digital I/O
RX					I	ST	EUSART asynchronous receive
DT					I/O	ST	EUSART synchronous data (see related TX/CK)

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
							PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when PSP module is enabled.
RD0/PSP0	19	38	38	**34**			
RD0					I/O	ST	Digital I/O
PSP0					I/O	TTL	Parallel Slave Port data
RD1/PSP1	20	39	39	**35**			
RD1					I/O	ST	Digital I/O
PSP1					I/O	TTL	Parallel Slave Port data
RD2/PSP2	21	40	40	**36**			
RD2					I/O	ST	Digital I/O
PSP2					I/O	TTL	Parallel Slave Port data
RD3/PSP3	22	41	41	**37**			
RD3					I/O	ST	Digital I/O
PSP3					I/O	TTL	Parallel Slave Port data
RD4/PSP4	27	2	2	**2**			
RD4					I/O	ST	Digital I/O
PSP4					I/O	TTL	Parallel Slave Port data
RD5/PSP5/P1B	28	3	3	**3**			
RD5					I/O	ST	Digital I/O
PSP5					I/O	TTL	Parallel Slave Port data
P1B					O	—	Enhanced CCP1 output
RD6/PSP6/P1C	29	4	4	**4**			
RD6					I/O	ST	Digital I/O
PSP6					I/O	TTL	Parallel Slave Port data
P1C					O	—	Enhanced CCP1 output
RD7/PSP7/P1D	30	5	5	**5**			
RD7					I/O	ST	Digital I/O
PSP7					I/O	TTL	Parallel Slave Port data
P1D					O	—	Enhanced CCP1 output

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

TABLE 1-3: PIC18F4XK20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP	UQFN			
							PORTE is a bidirectional I/O port
RE0/$\overline{RD}$/AN5	8	25	25	**23**			
RE0					I/O	ST	Digital I/O
$\overline{RD}$					I	TTL	Read control for Parallel Slave Port (see related $\overline{WR}$ and $\overline{CS}$ pins)
AN5					I	Analog	Analog input 5, ADC channel 5
RE1/$\overline{WR}$/AN6	9	26	26	**24**			
RE1					I/O	ST	Digital I/O
$\overline{WR}$					I	TTL	Write control for Parallel Slave Port (see related $\overline{CS}$ and $\overline{RD}$ pins)
AN6					I	Analog	Analog input 6, ADC channel 6
RE2/$\overline{CS}$/AN7	10	27	27	**25**			
RE2					I/O	ST	Digital I/O
$\overline{CS}$					I	TTL	Chip Select control for Parallel Slave Port (see related $\overline{RD}$ and $\overline{WR}$)
AN7					I	Analog	Analog input 7, ADC channel 7
RE3	—	—	—	**16**	—	—	See $\overline{MCLR}$/VPP/RE3 pin
VSS	12, 31	6, 30, 31	6, 29	**6,27**	P	—	Ground reference for logic and I/O pins
VDD	11, 32	7, 8, 28, 29	7, 28	**7,26**	P	—	Positive supply for logic and I/O pins
NC	—	13	12, 13, 33, 34	**—**	—	—	No connect

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Default assignment for CCP2 when Configuration bit CCP2MX is set.
2: Alternate assignment for CCP2 when Configuration bit CCP2MX is cleared.

6. Module: Device Features

The 40-pin UQFN package feature has been added to the PIC18F43/44/45/46K20 parts. The corrections are shown in **bold** in Table 1-1

TABLE 1-1: DEVICE FEATURES

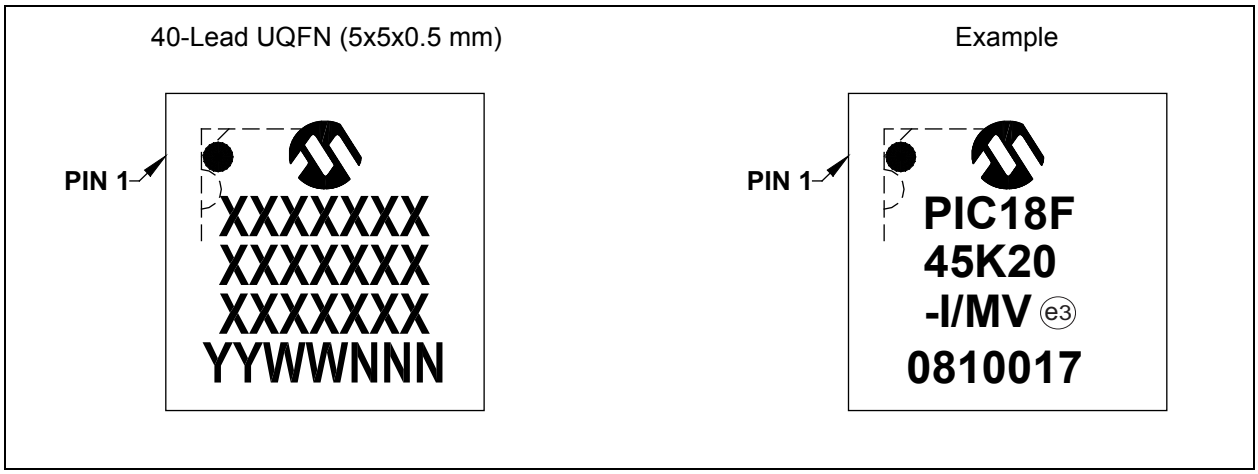
Features	PIC18F23K20	PIC18F24K20	PIC18F25K20	PIC18F26K20	PIC18F43K20	PIC18F44K20	PIC18F45K20	PIC18F46K20
Operating Frequency[(2)]	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz	DC – 64 MHz
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
Program Memory (Instructions)	4096	8192	16384	32768	4096	8192	16384	32768
Data Memory (Bytes)	512	768	1536	3936	512	768	1536	3936
Data EEPROM Memory (Bytes)	256	256	256	1024	256	256	256	1024
Interrupt Sources	19	19	19	19	20	20	20	20
I/O Ports	A, B, C, (E)[(1)]	A, B, C, (E)[(1)]	A, B, C, (E)[(1)]	A, B, C, (E)[(1)]	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
Timers	4	4	44		44		44	
Capture/Compare/PWM Modules	1	1	1	1	1	1	1	1
Enhanced Capture/ Compare/PWM Modules	1	1	11		11		11	
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	No	No	No	No	Yes	Yes	Yes	Yes
10-bit Analog-to-Digital Module	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 10 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels	1 internal plus 13 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/ Low-Voltage Detect	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	28-pin PDIP 28-pin SOIC 28-pin QFN 28-pin SSOP	40-pin PDIP 44-pin QFN 44-pin TQFP **40-pin UQFN**	40-pin PDIP 44-pin QFN 44-pin TQFP **40-pin UQFN**	40-pin PDIP 44-pin QFN 44-pin TQFP **40-pin UQFN**	40-pin PDIP 44-pin QFN 44-pin TQFP **40-pin UQFN**

Note 1: PORTE contains the single RE3 read-only bit. The LATE and TRISE registers are not implemented.

2: Frequency range shown applies to industrial range devices only. Maximum frequency for extended range devices is 48 MHz.

7. Module: Package Marking Information

The package marking information for the 40-pin UQFN is the following:



8. Module: Appendix B

The 40-pin UQFN package feature has been added to the PIC18F43/44/45/46K20 parts. The corrections are shown in **bold** in Table 1-1

TABLE 1-1: DEVICE DIFFERENCES

Features	PIC18F23K20	PIC18F24K20	PIC18F25K20	PIC18F26K20	PIC18F43K20	PIC18F44K20	PIC18F45K20	PIC18F46K20
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
Program Memory (Instructions)	4096	8192	16384	32768	4096	8192	16384	32768
Interrupt Sources	19	19	19	19	20	20	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/ PWM Modules	1	1	1	1	1	1	1	1
Enhanced Capture/Compare/ PWM Modules	1	1	1	1	1	1	1	1
Parallel Communications (PSP)	No	No	No	No	Yes	Yes	Yes	Yes
10-bit Analog-to-Digital Module	11 input channels	11 input channels	11 input channels	11 input channels	14 input channels	14 input channels	14 input channels	14 input channels
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin TQFP 44-pin QFN **40-pin UQFN**	40-pin PDIP 44-pin TQFP 44-pin QFN **40-pin UQFN**	40-pin PDIP 44-pin TQFP 44-pin QFN **40-pin UQFN**	40-pin PDIP 44-pin TQFP 44-pin QFN **40-pin UQFN**

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2008)

Initial release of this document.

Rev B Document (05/2009)

Updated Errata to new format; Added Module 11: PORTB and Module 12: ADC; minor edits.

Clarifications/Corrections to the Data Sheet: Added Module 1: MSSP; Module 2: Electrical Specifications; Module 3: Electrical Specifications.

Rev C Document (06/2009)

Clarifications/Corrections to the Data Sheet:

Deleted Module 1: MSSP: Figure 17-17 Baud Rate Generator Block Diagram, updating subsequent numbering. Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Rev D Document (11/2009)

Updated to add revision 0x1B.

Data Sheet Clarifications: Deleted Modules 1, 2, 3, 4, 5, 6.

Rev E Document (04/2010)

Updated to include early revisions of silicon, revision IDs 0xA through 0x11. These early revisions were described in DS80366 errata, which is now obsolete.

Rev F Document (05/2010)

Updated Table 1.

Rev G Document (07/2010)

Removed ADC Work around #2 and changed #3 to #2 (Module 28).

Rev H Document (07/2011)

Updated errata to the new format; Updated Module 16; Added Modules 38 and 39; Updated Table 2 to include the new modules.

Data Sheet Clarifications: Added Module 1.

Rev J Document (07/2012)

Added Silicon revision AF.

Rev K Document (05/2013)

Added MPLAB X IDE; Added Module 40, Low-Voltage Detect.

Data Sheet Clarifications: Added Module 2, Electrical Characteristics.

Rev L Document (12/2013)

Data Sheet Clarification: Updated Module 2 (Electrical Characteristics, Table 26-8).

Rev M Document (4/2014)

Data Sheet Clarifications: Added Modules 3, 4, 5, 6, 7, 8.

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